



**PATENT**

**THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re Application of:**

Pan et al.

**Serial No.:** Not yet assigned

**Filed:** July 12, 2000

**For:** TECHNIQUE FOR ELIMINATION  
OF PITTING ON SILICON SUBSTRATE  
DURING GATE STACK ETCH

**Examiner:** Unknown

**Group Art Unit:** Unknown

**Attorney Docket No.:** 2915.3US  
(96-0149.2)

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**INFORMATION DISCLOSURE STATEMENT**

Box PATENT APPLICATION  
Commissioner for Patents  
Washington, D.C. 20231

Sir:

The present application is a continuation of application Serial No. 09/073,494, filed May 6, 1998, pending, which is a divisional of application Serial No. 08/682,935, filed July 16, 1996, now U.S. Patent 6,087,254, issued July 11, 2000.

Pursuant to M.P.E.P. 2001.06(b), the Examiner is respectfully requested to consider the information of record in the prior applications, and to confirm in the first Office Action on the merits that such art has in fact been reviewed. A PTO-1449 form listing all of the information of record in the prior applications is enclosed herewith.

Attorney Docket No. 2915.3US (96-0149.2)

This Information Disclosure Statement is filed within three (3) months of the filing date of the above-identified application, and no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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Enclosure: Form PTO-1449

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